1	Application No.	Applicant(s)
Notice of Allowability	09/693,976 Examiner	CASAVANT ET AL. Art Unit
	Lammer	Artonit
	Aaron C Perez-Daple	2154
The MAILING DATE of this communication appear All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RI	(OR REMAINS) CLOSED in this apport or other appropriate communication (GHTS. This application is subject to	plication. If not included n will be mailed in due course. THIS
1. A This communication is responsive to RCE filed 12/16/04.		
2. ☑ The allowed claim(s) is/are <u>1-13,17 and 19-47</u> .		
3. The drawings filed on <u>06 May 2004 and 23 October 2000</u> a	are accepted by the Examiner.	
 4. ☐ Acknowledgment is made of a claim for foreign priority una) ☐ All b) ☐ Some* c) ☐ None of the: 1. ☐ Certified copies of the priority documents have 2. ☐ Certified copies of the priority documents have 3. ☐ Copies of the certified copies of the priority documents have International Bureau (PCT Rule 17.2(a)). 	been received. been received in Application No	
* Certified copies not received:		
Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDONM THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.	of this communication to file a reply ENT of this application.	complying with the requirements
5. A SUBSTITUTE OATH OR DECLARATION must be submit INFORMAL PATENT APPLICATION (PTO-152) which give	itted. Note the attached EXAMINER is reason(s) why the oath or declara	'S AMENDMENT or NOTICE OF tion is deficient.
 CORRECTED DRAWINGS (as "replacement sheets") mus (a) ☐ including changes required by the Notice of Draftspers 1) ☐ hereto or 2) ☐ to Paper No./Mail Date (b) ☐ including changes required by the attached Examiner's Paper No./Mail Date Identifying indicia such as the application number (see 37 CFR 1. 	on's Patent Drawing Review (PTO- s Amendment / Comment or in the C	Office action of
each sheet. Replacement sheet(s) should be labeled as such in the	•	
7. DEPOSIT OF and/or INFORMATION about the deposit attached Examiner's comment regarding REQUIREMENT I	sit of BIOLOGICAL MATERIAL n FOR THE DEPOSIT OF BIOLOGIC <i>i</i>	nust be submitted. Note the AL MATERIAL.
Attachment(s)		
1. Notice of References Cited (PTO-892)	5. Notice of Informal P	atent Application (PTO-152)
2. Notice of Draftperson's Patent Drawing Review (PTO-948)	6. Interview Summary	
3. Information Disclosure Statements (PTO-1449 or PTO/SB/0	Paper No./Mail Dat 8), 7. ⊠ Examiner's Amendn	
Paper No./Mail Date4. Examiner's Comment Regarding Requirement for Deposit	8. X Examiner's Stateme	nt of Reasons for Allowance
of Biological Material	9. Other	
JOHN FOLLANSBEE SUPERVECTY PATENT EXAMINER TECHNOLOGY CENTER 2100		

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EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Natalya Dvorson on 3/31/05.

- 2. Claims 1-13, 17, and 19-47 as amended below are allowed.
- 3. Claims 14-16 and 18 remain cancelled by Applicant.
- 4. The Application has been amended as follows:

In the claims:

1. (currently amended): A method of verification for a design, comprising: providing a description of said design;

specifying correctness criteria for said design, wherein said correctness criteria are expressed as one or more correctness properties;

abstracting said design description to provide an abstract model of said design; generating a witness graph for said one or more correctness properties based on a deterministic analysis of said abstract model where the deterministic analysis serves to modify the abstract model by over-approximating-iteratively refining and pruning states and transitions which capture all witnesses or counterexamples demonstrating said one or more correctness properties; and

where when the deterministic analysis does not produce a conclusive result, generating a testbench automatically from said witness graph for performing simulation with said testbench, where the testbench generates simulation test vectors for the simulation that target the over-approximated states and transitions in the witness graph when searching for a concrete witness or counterexample with respect to said correctness criteria.

- 19. (currently amended): The method for verification as set forth in claim 1, wherein said deterministic analysis comprises using symbolic model checking on the abstract model to identify the over-approximated states and transitions which capture all witnesses or counterexamples demonstrating the correctness properties.
- 24. (currently amended): The method for verification as set forth in claim 1, wherein said deterministic analysis comprises using constraint solving on the abstract model to identify the over-approximated states and transitions which capture all witnesses or counterexamples demonstrating said one or more correctness properties.
- 28. (currently amended): A device-readable medium comprising program instructions for causing the device to perform verification for a design, comprising:

receiving an abstract model of said design, said abstract model abstracted from a design description of said design;

receiving one or more correctness properties representing correctness criteria specified for said design;

generating a witness graph for said one or more correctness properties based on a deterministic analysis of said abstract model where the deterministic analysis serves to

modify the abstract model by over-approximating iteratively refining and pruning states and transitions which capture all witnesses or counterexamples demonstrating said one or more correctness properties; and

where when the deterministic analysis does not produce a conclusive result, automatically generating a testbench from said witness graph for performing simulation with said testbench, where the testbench generates simulation test vectors for the simulation that target the over-approximated states and transitions in the witness graph when searching for a concrete witness or counterexample with respect to said correctness criteria.

- 29. (currently amended): The device-readable medium as set forth in claim 28, wherein said deterministic analysis comprises using symbolic model checking on the abstract model to identify the over-approximated states and transitions which capture all witnesses or counterexamples demonstrating the correctness properties.
- 34. (currently amended): The device-readable medium as set forth in claim 28, wherein said deterministic analysis comprises using constraint solving on the abstract model to identify the over-approximated states and transitions which capture all witnesses or counterexamples demonstrating said one or more correctness properties.
- 38. (currently amended): An apparatus for verification of a design comprising: an input module for receiving an abstract model of said design, said abstract model abstracted from a design description of said design, and for receiving one or more correctness properties representing correctness criteria specified for said design;

a witness graph module for generating a witness graph for said one or more correctness properties based on a deterministic analysis of said abstract model where when the deterministic analysis serves to modify the abstract model by overapproximating iteratively refining and pruning states and transitions which capture all witnesses or counterexamples demonstrating the correctness properties; and

a testbench module for generating a testbench automatically from said witness graph for performing simulation with said testbench, where the testbench generates simulation test vectors for the simulation that target the over approximated states and transitions in the witness graph when searching for a concrete witness or counterexample with respect to said correctness criteria.

- 39. (currently amended): The apparatus as set forth in claim 38, wherein said deterministic analysis comprises using symbolic model checking on the abstract model to identify the over-approximated states and transitions which capture all witnesses or counterexamples demonstrating the correctness properties.
- 44. (currently amended): The apparatus as set forth in claim 38, wherein said deterministic analysis comprises using constraint solving on the abstract model to identify the over-approximated states and transitions which capture all witnesses or counterexamples demonstrating the correctness properties.
- 5. The following is an examiner's statement of reasons for allowance: with respect to independent claims 1, 28, and 38, the prior art of record does not teach or suggest a system and method of verification for a design having the recited features and further comprising performing a deterministic analysis to modify the abstract model by iteratively refining and

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pruning states and transitions which capture all witnesses or counterexamples demonstrating said one or more correctness properties. Therefore, the present invention teaches an improved method and system of verification for a design.

With respect to independent claim 17, the prior art of record does not teach or suggest a method of assessing simulation coverage of a set of given simulation vectors for a design comprising the specifically recited steps for modifying and pruning the abstract model for generating a witness graph. Therefore, the present invention teaches an improved method for of assessing simulation coverage of a set of given simulation vectors for a design.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron C Perez-Daple whose telephone number is (571) 272-3974. The examiner can normally be reached on 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on (571) 272-3964. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent
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(toll-free).

JA 4/3/05

Aaron Perez-Daple

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